CLAIMS

What is claimed is:

1. A method of forming a probe card comprising:

providing a substrate having a first surface and a second surface;

disposing a plurality of conductive traces adjacent at least one of the first surface and the second surface;

providing a plurality probe elements in electrical communication with the plurality of conductive traces; and

providing a plurality of fuse elements in respective electrical communication with at least some of the plurality of conductive traces, at least some of the plurality of fuse elements disposed immediately adjacent at least one of the first surface and the second surface.

2. The method of claim 1, wherein said providing a plurality of fuse elements comprises providing a fuse element of the plurality of fuse elements in respective electrical communication with substantially each of the plurality of conductive traces.

3. The method of claim 1, wherein said providing a plurality of fuse elements comprises providing at least one fuse of the plurality of fuse elements configured to be replaceable or repairable after being tripped.

4. The method of claim 3, wherein the at least one fuse element of the plurality of fuse elements is formed of a material selected from the group consisting of titanium tungsten, aluminum, platinum silicide, copper, nichrome, doped polysilicon, metal silicide, and alloys of any thereof.

5. The method of claim 3, wherein said providing a plurality of fuse elements comprises forming at least some of the plurality of fuse elements using a deposition process.

6. The method of claim 3, further comprising constructing at least some of the plurality of conductive traces and at least some of the plurality of fuse elements at substantially the same time and by a single deposition process.

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7. The method of claim 3, further comprising providing a plurality of test contacts adjacent at least one of the first surface and the second surface, at least some of the test contacts in electrical communication with respective conductive traces of the plurality of conductive traces, and further comprising forming each of the plurality of conductive traces, the plurality of fuse elements, and the plurality of test contacts of the same materials.

8. The method of claim 1, wherein said providing a plurality of fuse elements comprises inserting at least one of the plurality of fuse elements in through-hole portions configured in at least one of the first surface and the second surface of the substrate.

9. The method of claim 1, wherein said providing a plurality of fuse elements comprises providing at least one of the plurality of fuse elements configured as a dual in-line pin header fuse.

10. The method of claim 1, wherein said providing a plurality of fuse elements comprises providing at least one of the plurality of fuse elements configured as a dual in-line socket fuse.

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11. The method of claim 1, wherein at least one fuse of the plurality of fuse elements is configured to be self-resetting after being tripped.

12. The method of claim 11, wherein the at least one fuse is configured as a PPTC fuse.

13. The method of claim 11, wherein the at least one fuse is configured as a bimetallic switch.

14. A method of fabricating a probe card comprising:

providing a probe card substrate;

providing a plurality of conductive traces adjacent a surface of said probe card substrate;

providing a plurality of probe elements in electrical communication with the plurality of conductive traces, at least one probe element of the plurality of probe elements configured for supplying a test signal to at least one semiconductor die; and

providing at least one repairable or replaceable fuse component in electrical communication with at least one of the plurality of conductive traces.

15. The method of claim 14, further comprising providing a test contact in electrical communication with at least one conductive trace of the plurality of conductive traces, and further comprising providing a pogo pin in electrical communication with the test contact, wherein the at least one repairable or replaceable fuse component is configured as a portion of the pogo pin.

16. The method of claim 14, wherein said providing a plurality of probe elements comprises providing the plurality of probe elements in a configuration adapted to be temporarily electrically coupled with a semiconductor wafer having a plurality of electrical contacts thereon.

17. The method of claim 16, wherein said providing a plurality of probe elements comprises arranging conductive tips of the plurality of probe elements in a mirror image of a pattern of the plurality of electrical contacts on the semiconductor wafer.

18. The method of claim 16, wherein said providing a probe card substrate includes providing the probe card substrate with a coefficient of thermal expansion which substantially matches a coefficient of thermal expansion of the semiconductor wafer.

19. The method of claim 14, wherein said providing at least one repairable or replaceable fuse component comprises providing an active fuse.

20. The method of claim 14, wherein said providing at least one repairable or replaceable fuse component comprises providing a passive fuse.

21. The method of claim 20, further comprising providing a plurality of test contacts in electrical communication with respective conductive traces of the plurality of conductive traces, and wherein providing a passive fuse comprises providing a passive fuse configured as a cutout portion of at least one test contact of the plurality of test contacts.

22. A method of using a probe card for testing at least one semiconductor die, comprising:

providing a probe card having a plurality of probe elements connected thereto, the plurality of probe elements configured for supplying test signals to the at least one semiconductor die;

providing a plurality of fuses in electrical communication with at least some of the probe elements; and

testing the at least one semiconductor die by supplying test signals to the at least one semiconductor die through the fuse.

23. The method of claim 22, further comprising repairing or replacing a fuse of the plurality of fuses if the fuse has been tripped by a test signal.

24. The method of claim 23, wherein said replacing the fuse comprises inserting a new fuse in through-hole portions of a surface of the probe card.

25. The method of claim 23, wherein said repairing the fuse comprises forming new portions of the fuse by a deposition technique.

26. A probe card comprising:

a substrate having a first surface and a second surface;

a plurality of conductive traces disposed adjacent at least one of the first surface and the second

surface;

a plurality of probe elements in respective electrical communication with the plurality of conductive traces; and

a plurality of fuses disposed adjacent at least one of the first surface and the second surface and in respective electrical communication with the plurality of conductive traces.

27. The probe card of claim 26, wherein at least one fuse of the plurality of fuses is configured to be replaceable or repairable after being tripped by an electrical current supplied thereto.

28. The probe card of claim 26, wherein at least one fuse of the plurality of fuses is configured of a material selected from the group consisting of titanium tungsten, aluminum, platinum silicide, copper, nichrome, doped polysilicon, metal silicide, and alloys of any thereof.

29. The probe card of claim 26, wherein at least one of plurality of fuses and at least one of the plurality of conductive traces are constructed of the same materials.

30. The probe card of claim 26, wherein at least one of plurality of fuses and at least one of the plurality of conductive traces are constructed over a surface of the probe card during a single deposition process.

31. The probe card of claim 26, wherein each of the plurality of fuses are fabricated of the same materials in a single deposition process.

32. The probe card of claim 26, wherein at least one fuse of the plurality of fuses is configured as a dual in-line pin header fuse.

33. The probe card of claim 26, wherein at least one fuse of the plurality of fuses is configured as a dual in-line socket fuse.

34. The probe card of claim 26, wherein at least one fuse of the plurality of fuses is configured to be self-resetting after being tripped.

35. The probe card of claim 34, wherein the at least one fuse is configured as a PPTC fuse.

36. The probe card of claim 34, wherein the at least one fuse is configured as a bimetallic switch.

37. The probe card of claim 26, wherein at least one fuse of the plurality of fuses is configured as a passive fuse.

38. The probe card of claim 26, wherein each of the plurality of conductive traces is in electrical communication with a respective fuse of the plurality of fuses.

39. The probe card of claim 26, wherein each of the plurality of fuses is disposed adjacent a peripheral region of the substrate.

40. The probe card of claim 26, wherein the probe card is configured as a probe card selected from the group consisting of vertical contact probe cards, cantilever-type probe cards, and probe cards for wafer level burn-in.

41. The probe card of claim 26, further comprising at least one electrical component selected from the group consisting of resistors, transistors, capacitors, and diodes in electrical communication with at least one conductive trace of the plurality of conductive traces.

42. The probe card of claim 26, wherein at least one fuse of the plurality of fuses is configured as a discrete electrical component.

43. The probe card of claim 42, wherein the discrete electrical component is affixed in a surface mount configuration to a portion of the probe card.

44. The probe card of claim 42, wherein the discrete electrical component is mounted by conductive pins into through-hole portions of a surface of the probe card.

45. The probe card of claim 26, wherein at least one conductive trace of the plurality of conductive traces is disposed in a layer proximately underneath at least one of the first surface and second surface of the substrate.

46. The probe card of claim 26, wherein at least one fuse of the plurality of fuses is located directly adjacent a probe element of the plurality of probe elements.

47. The probe card of claim 26, wherein each fuse of the plurality of fuses is in electrical communication with a respective probe element of the plurality of probe elements.

48. The probe card of claim 26, wherein the plurality of probe elements are configured in a pattern for simultaneously testing integrated circuitry of a plurality of semiconductor dice.

49. The probe card of claim 26, further comprising a test contact in electrical communication with a conductive trace of the plurality of conductive traces, the test contact configured for supplying a current to the conductive trace, and wherein at least one fuse of the plurality of fuses is interposed adjacently between the test contact and the conductive trace.

50. A semiconductor die testing system comprising:

a probe card including:

a substrate having a first surface and a second surface;

a plurality of conductive traces disposed adjacent at least one of the first surface and the second surface;

a plurality of probe elements in electrical communication with the plurality of conductive

traces;

a plurality of fuses disposed adjacent at least one of the first surface and the second surface, the plurality of fuses in electrical communication with the plurality of conductive traces; and

semiconductor device testing apparatus linkable with the probe card, the semiconductor testing apparatus configured for sending test signals through the probe card.

51. The semiconductor die testing system of claim 50, further comprising a pogo pin interfacing the probe card and the semiconductor device testing apparatus, and wherein a portion of the pogo pin is configured as a protective fuse in electrical communication with the probe card.

52. The semiconductor die testing system of claim 50, wherein the probe card is configured as a needle-type probe card.

53. The semiconductor die testing system of claim 50, wherein the probe card is configured as a membrane-type probe card.

54. The semiconductor die testing system of claim 50, wherein the probe card is configured as a probe card selected from the group consisting of vertical contact probe cards, cantilever-type probe cards, and probe cards for wafer level burn-in.

55. The semiconductor die testing system of claim 50, wherein the probe card is configured for the testing of a plurality of semiconductor dice at once.